ABSTRACT OF THE DISCLOSURE

A column read amplifier power-gating technique for DRAM devices and those devices incorporating embedded DRAM which incorporate a power-down (or Sleep) mode of operation which overcomes the deficiencies of conventional power-gating approaches by eliminating the need for a large, separate power-gating transistor thereby saving on-chip area yet still reducing power during Sleep Mode. In operation, the column select signal YR is controlled such that it is driven below VSS during Sleep Mode when N-channel pass transistors are used in the column read amplifier or to a supply voltage level of VCC when P-channel devices are used instead. This significantly reduces the current through the pass transistors and yet causes no reduction in the switching speed of the column read amplifiers.